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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,654	09/24/2001	Koji Motoyama	914-138	5562

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EXAMINER	
ENG, GEORGE	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,654	MOTOYAMA, KOJI	
	Examiner	Art Unit	
	George Eng	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 10/22/2004. Accordingly, claims 2-3 are canceled and claims 1 and 4 are pending for examination.

Information Disclosure Statement

2. The information disclosure statement filed 10/22/2004 has been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art in the specification and Shimotashiro et al. (US PAT. 5,361,043 hereinafter Shimotashiro).

Regarding claim 1, Applicant admitted prior art in the specification discloses a low noise down-converter for satellite broadcast receiving comprising a mixer converting a received high frequency signal into an intermediate-frequency signal (page 1, lines 10-15), the mixer including a transistor (50, figure 9) for performing frequency conversion, a PNP bipolar transistor (Tr1,

figure 9) having an emitter connected to a drain of said transistor and a collector connected to a gate of said transistor (page 1, lines 26-30). Applicant's admitted prior art in the specification differs from the claimed invention in not specifically teaching a temperature characteristic compensating circuit connected to a base of the PNP bipolar transistor and canceling a temperature characteristic of the PNP bipolar transistor, wherein the temperature characteristic compensating circuit includes an NPN bipolar transistor having a conductive terminal connected to the base of the PNP bipolar transistor and the PNP and NPN bipolar transistors are packaged into a dual transistor. However, Shimotashiro teaches a circuit provided with NPN type transistor (Q_{21}, figure 4) having a conductive terminal connected to the base of PNP type transistor (Q_{31}, figure 4), which the PNP and the NPN transistors are packaged into a dual transistor in order to compensate for the temperature dependence of constructional elements by equalizing voltage applied to an output terminal with the direct current bias voltage applied to the bias of the NPN type transistor (col. 12 line 43 through col. 15 line 56). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Applicant admitted prior art in having the temperature characteristic compensating circuit connected to the base of the PNP bipolar transistor and canceling the temperature characteristic of the PNP bipolar transistor, wherein the temperature characteristic compensating circuit includes an NPN bipolar transistor having a conductive terminal connected to the base of the PNP bipolar transistor and the PNP and NPN bipolar transistors are packaged into a dual transistor, as per teaching of Shimotashiro, because it compensates for the temperature dependence of constructional elements.

Regarding claim 4, Applicant admitted prior art in the specification discloses a mixer (page 1, lines 10-15) comprising a transistor (50, figure 9) for performing frequency conversion, a PNP bipolar transistor (Tr1, figure 9) having an emitter connected to a drain of said transistor and a collector connected to a gate of said transistor (page 1, lines 26-30). Applicant's admitted prior art in the specification differs from the claimed invention in not specifically teaching a temperature characteristic compensating circuit for canceling a temperature characteristic of the PNP bipolar transistor including an NPN bipolar transistor having a conductive terminal connected to the base of the PNP bipolar transistor and the PNP and NPN bipolar transistors are packaged into a dual transistor. However, Shimotashiro teaches a circuit provided with NPN type transistor (Q_{21}, figure 4) having a conductive terminal connected to the base of PNP type transistor (Q_{31}, figure 4), which the PNP and the NPN transistors are packaged into a dual transistor in order to compensate for the temperature dependence of constructional elements by equalizing voltage applied to an output terminal with the direct current bias voltage applied to the bias of the NPN type transistor (col. 12 line 43 through col. 15 line 56). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Applicant admitted prior art in having the temperature characteristic compensating circuit for canceling a temperature characteristic of the PNP bipolar transistor including an NPN bipolar transistor having a conductive terminal connected to the base of the PNP bipolar transistor and the PNP and NPN bipolar transistors are packaged into a dual transistor, as per teaching of Shimotashiro, because it compensates for the temperature dependence of constructional elements.

Response to Arguments

5. Applicant's arguments with respect to claims 1 and 4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Okuma et al. (US PAT. 6,054,898) discloses a semiconductor device capable of maintaining good temperature compensation and reducing manufacture costs of SEPP connecting NPN and PNP power transistors and temperature compensating and biasing circuit (figure 10 and col. 19 line 23 through col. 21 line 10).

Rossi et al. (US PAT. 5,578,956) discloses a circuit for limiting the maximum current to be supplied to a load by providing a circuit contains an NPN transistor (Q_{270}, figure 4) having a conductive terminal connected to a base of a PNP transistor (Q_6, figure 4).

Price (US PAT. 4,163,908) discloses a bias circuit for complementary transistor (col. 3 line 42 through col. 4 line 59).

Sato (US PAT. 3,701,910) discloses a compensation circuit for voltage and temperature in a transistor circuit having an NPN type transistor and a PNP type transistor with its base connected to the collector of the NPN transistor (abstract).

Tanaka (JP 01160186A) discloses an impedance conversion circuit being formed by the combination of NPN and PNP transistors to make the clamp level stable (abstract).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Eng whose telephone number is 703-308-9555. The examiner can normally be reached on Tue-Fri 7:30 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A. Kuntz can be reached on 703-305-4708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Eng
Primary Examiner
Art Unit 2643